OIPE JC67 APR C 5 2004 PATENT & TRADEMARK OFFICE

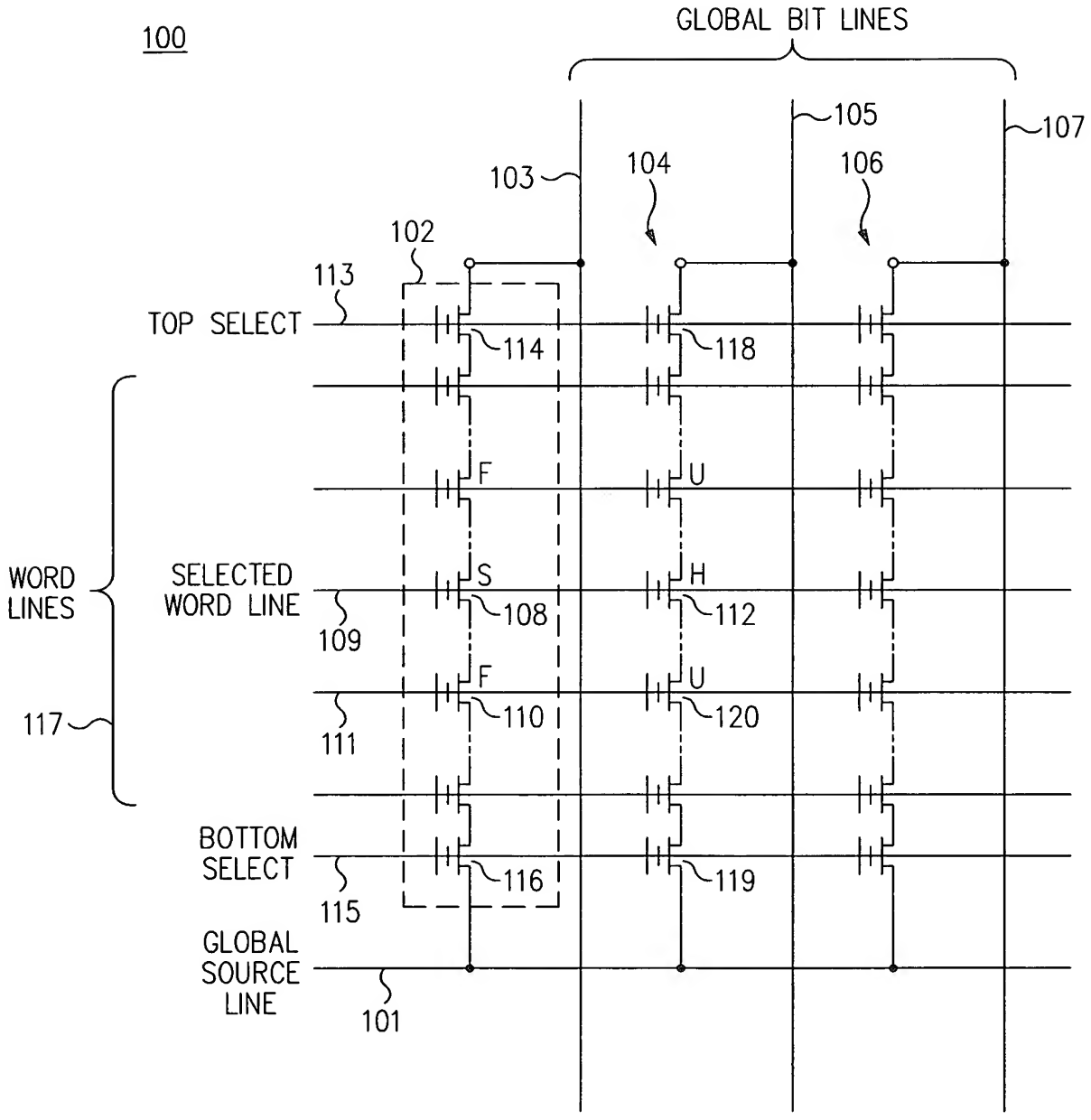

FIG. 1

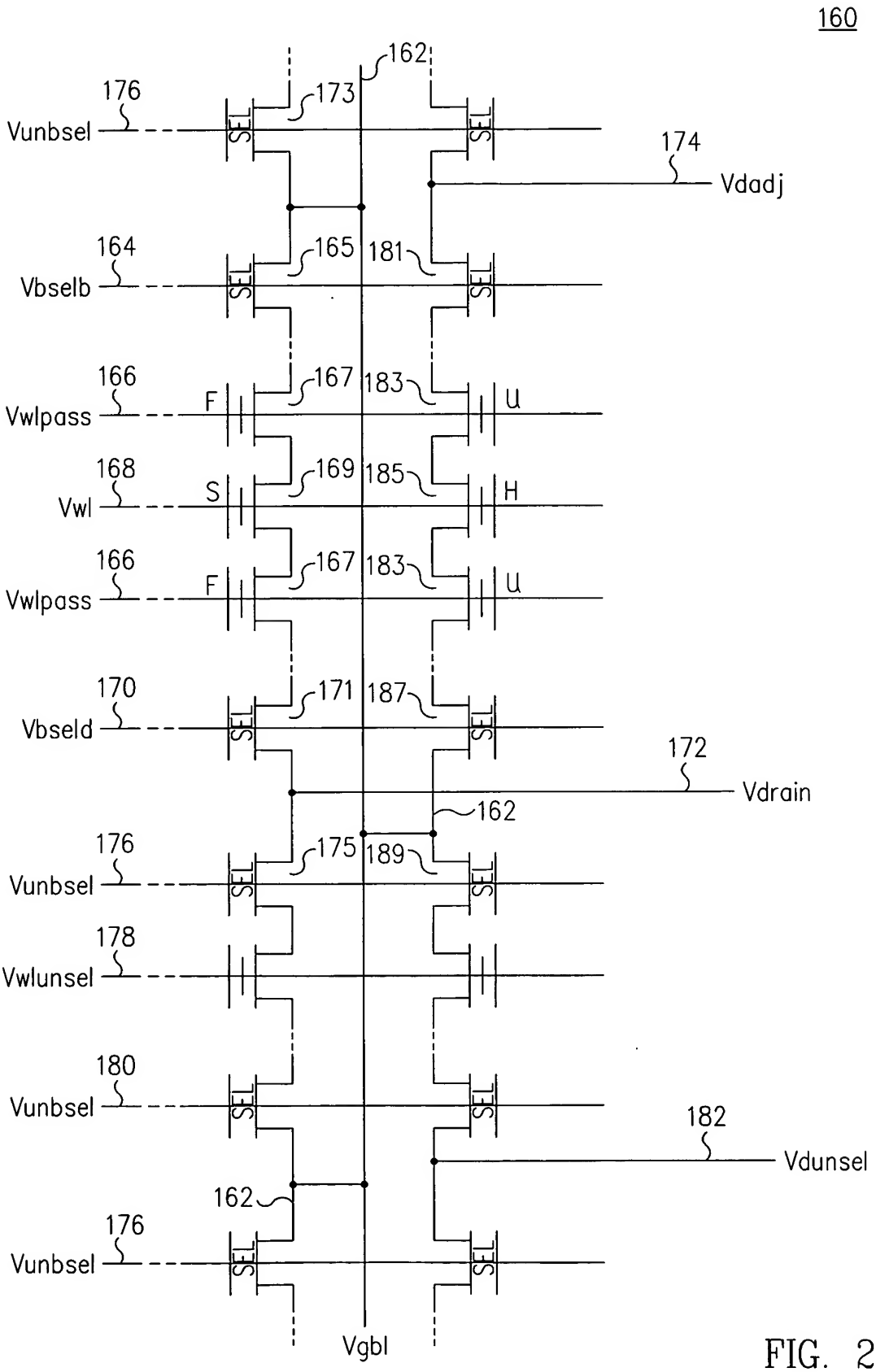
160
162
176
Vunbsel
173
SEL
174
Vdadj
164
Vbselb
165
181
166
Vwlpass
F
167
183
U
168
Vwl
S
169
185
H
166
Vwlpass
F
167
183
U
170
Vbseld
171
187
172
Vdrain
162
176
Vunbsel
175
189
178
Vwlunsel
180
Vunbsel
182
Vdunsel
162
176
Vunbsel
Vgbl

FIG. 2

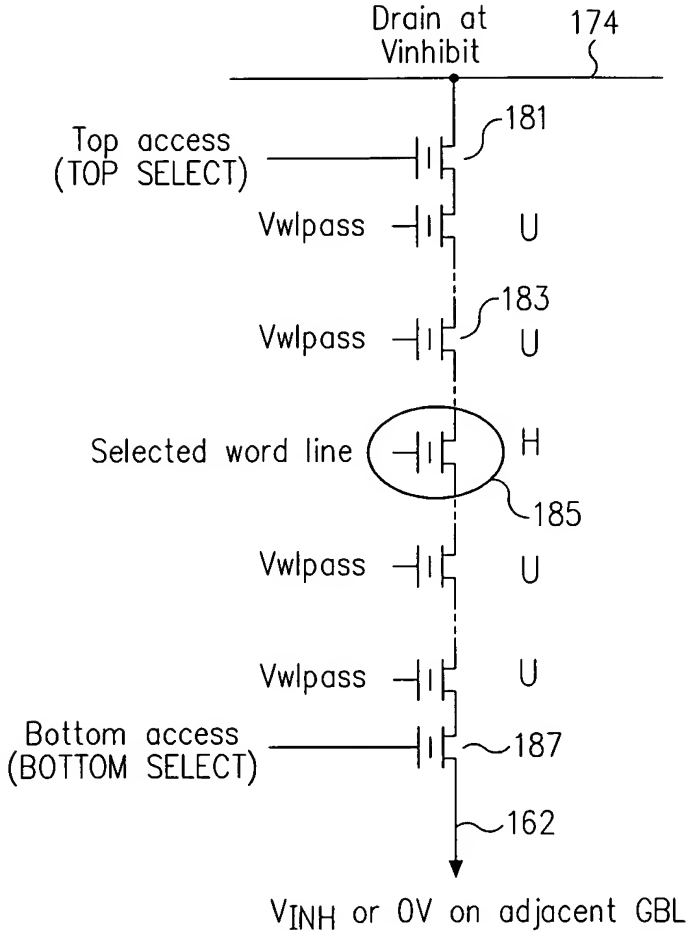
Drain at
Vinhibit
174
181
Top access
(TOP SELECT)
Vwlpass
U
183
Vwlpass
U
Selected word line
H
185
Vwlpass
U
Vwlpass
U
Bottom access
(BOTTOM SELECT)
187
162
V_{INH} or 0V on adjacent GBL

FIG. 3

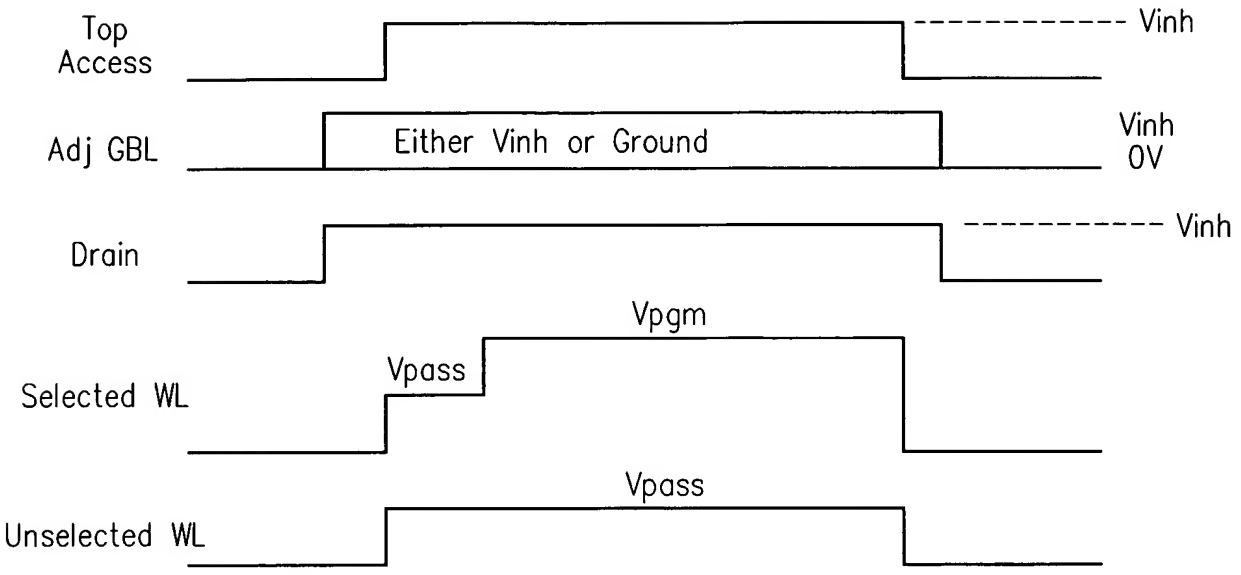
Top Access
Vinh
Adj GBL
Either Vinh or Ground
Vinh
0V
Drain
Vinh
Vpgm
Vpass
Selected WL
Vpass
Unselected WL

FIG. 4

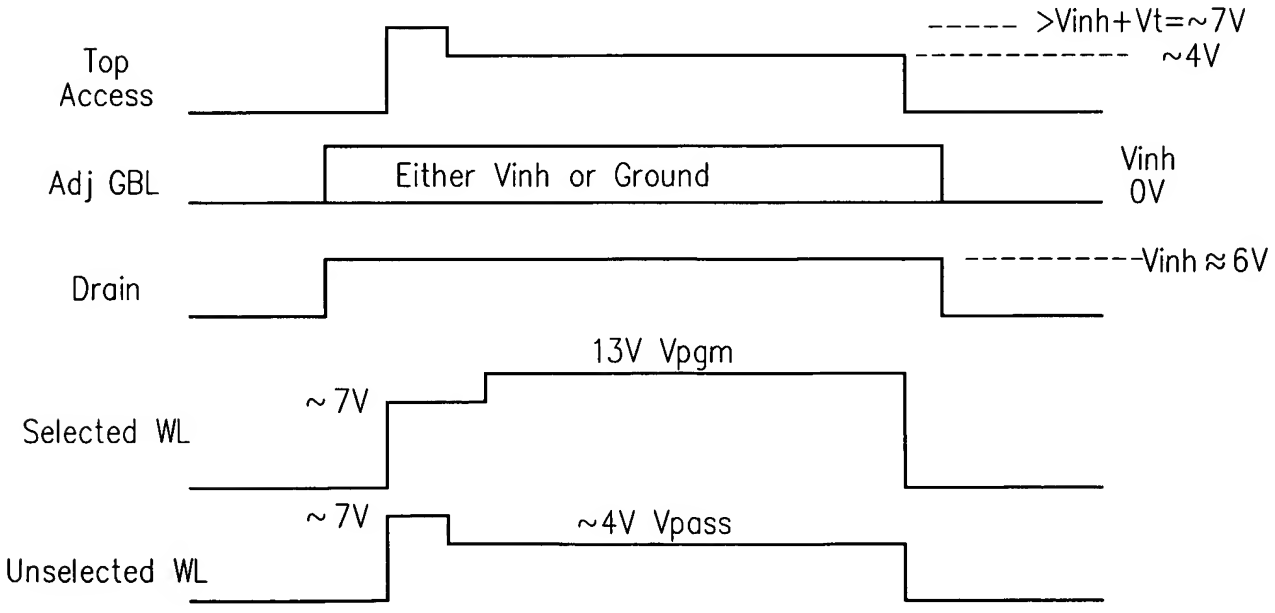
>Vinh+Vt=~7V
Top Access
~4V
Adj GBL
Either Vinh or Ground
Vinh
0V
Drain
Vinh ≈ 6V
13V Vpgm
~7V
Selected WL
~7V
~4V Vpass
Unselected WL

FIG. 5

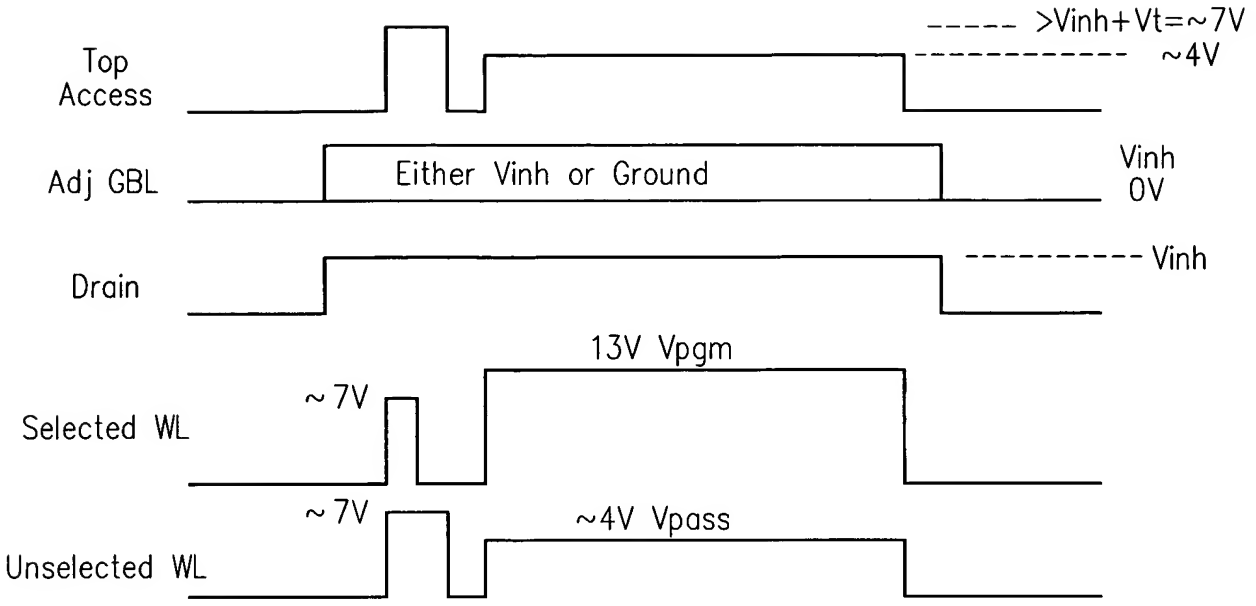
----- >Vinh+Vt=~7V
~4V
Top Access
Adj GBL
Either Vinh or Ground
Vinh
0V
Drain
Vinh
13V Vpgm
~7V
Selected WL
~7V
~4V Vpass
Unselected WL

FIG. 6

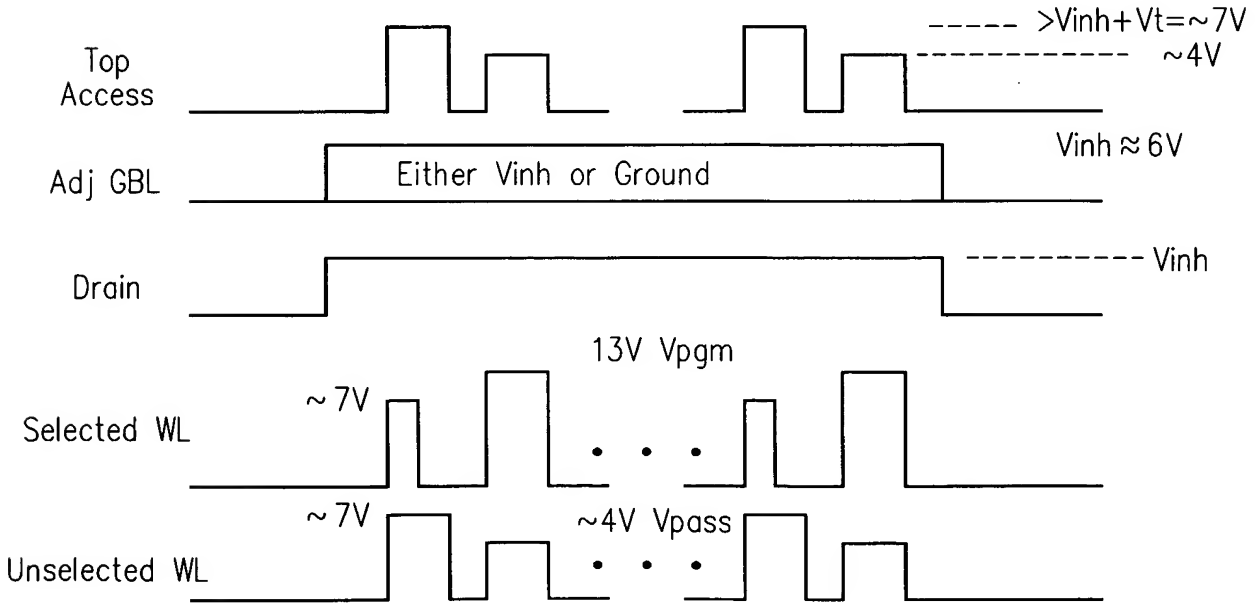
----- >Vinh+Vt=~7V
~4V
Top Access
Vinh ≈ 6V
Adj GBL
Either Vinh or Ground
Drain
Vinh
13V Vpgm
~7V
Selected WL
~7V
~4V Vpass
Unselected WL

FIG. 7

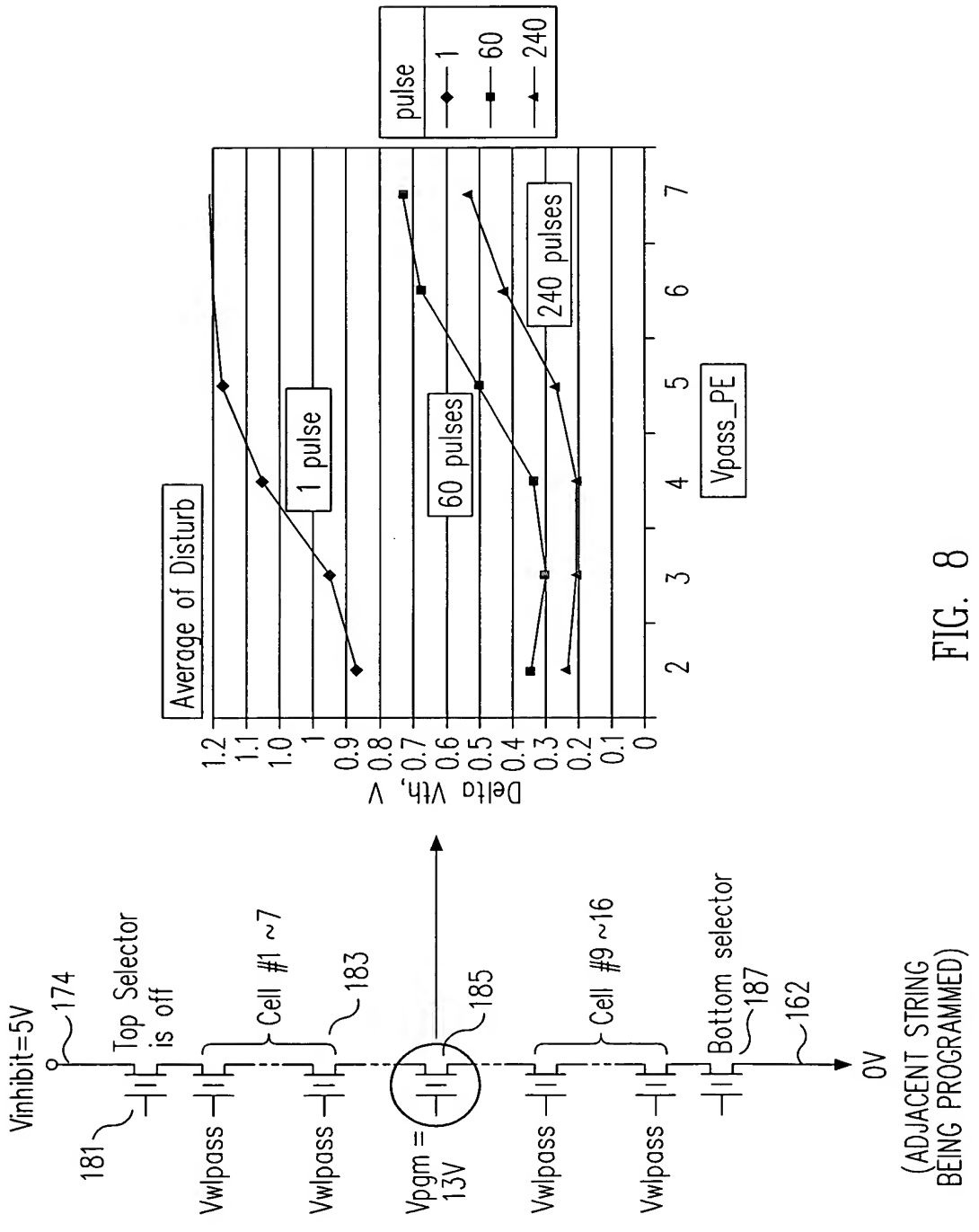
Vinhibit=5V
174
Top Selector is off
181
Vwlpass
Cell #1 ~7
183
Vwlpass
Vpgm = 13V
185
Vwlpass
Cell #9 ~16
Vwlpass
Bottom selector
187
162
0V
(ADJACENT STRING BEING PROGRAMMED)
Delta Vth, V
Average of Disturb
1 pulse
60 pulses
240 pulses
Vpass_PE
pulse
1
60
240

FIG. 8

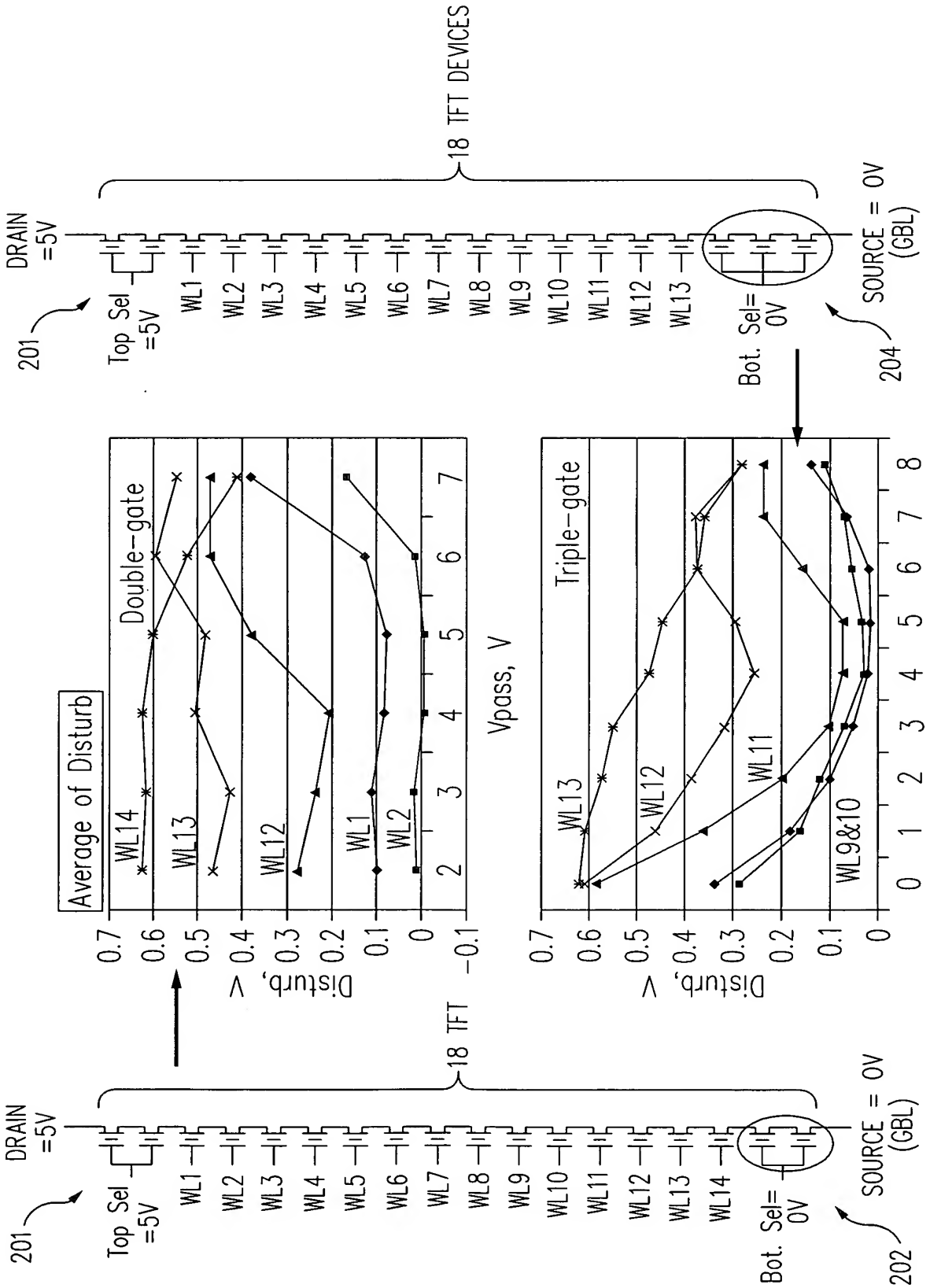
18 TFT DEVICES
DRAIN =5V
201
Top Sel =5V
WL1
WL2
WL3
WL4
WL5
WL6
WL7
WL8
WL9
WL10
WL11
WL12
WL13
Bot. Sel= 0V
204
SOURCE = 0V (GBL)
Average of Disturb
Double-gate
Triple-gate
WL14
WL13
WL12
WL1
WL2
WL11
WL9&10
Disturb, V
Vpass, V
18 TFT
202

FIG. 9

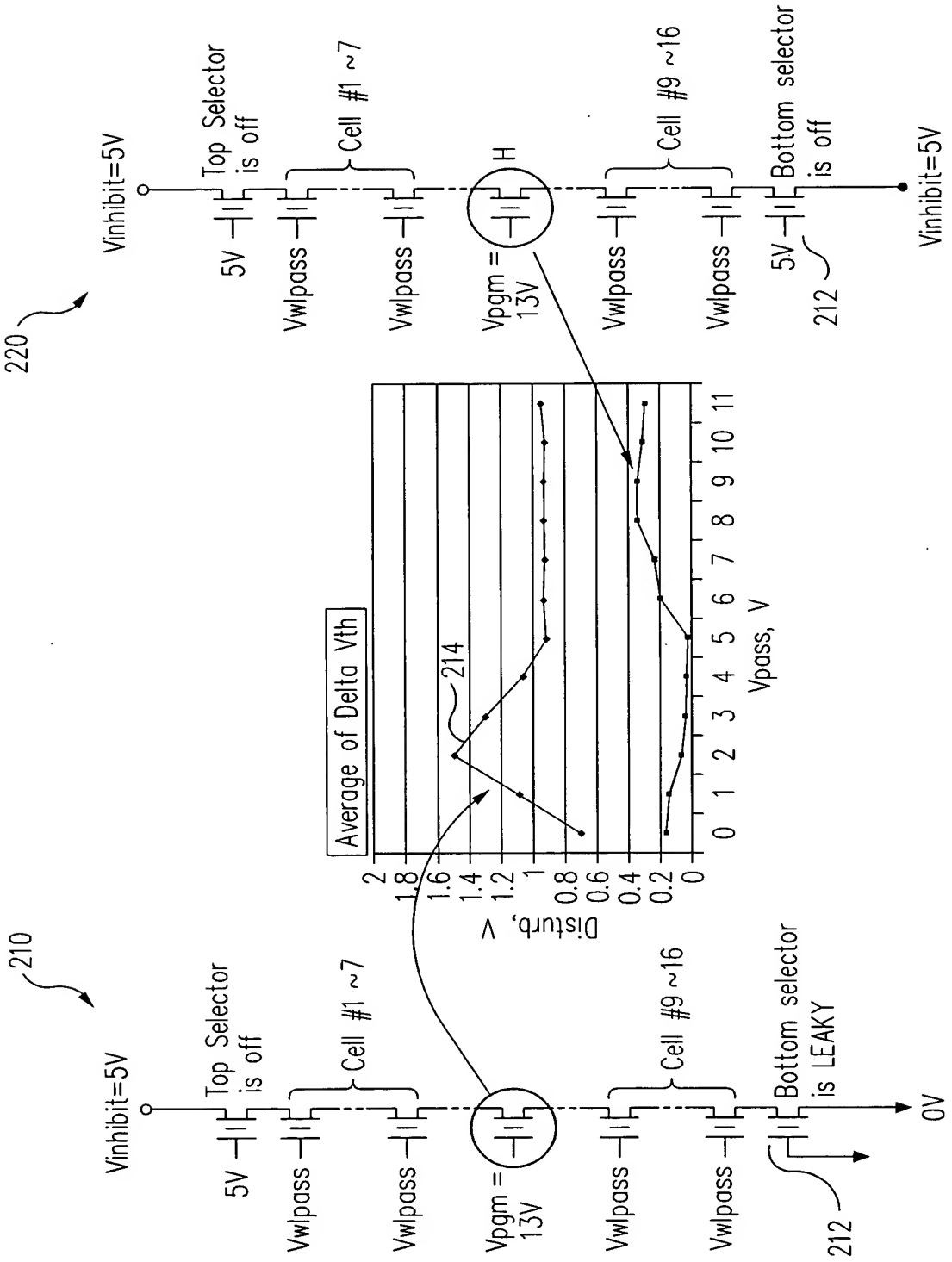
210
220
Vinhibit=5V
Top Selector is off
5V
Vwlpass
Cell #1 ~7
Vpgm = 13V
Cell #9 ~16
Bottom selector is LEAKY
0V
212
Bottom selector is off
Average of Delta Vth
Disturb, V
Vpass, V
214

FIG. 10

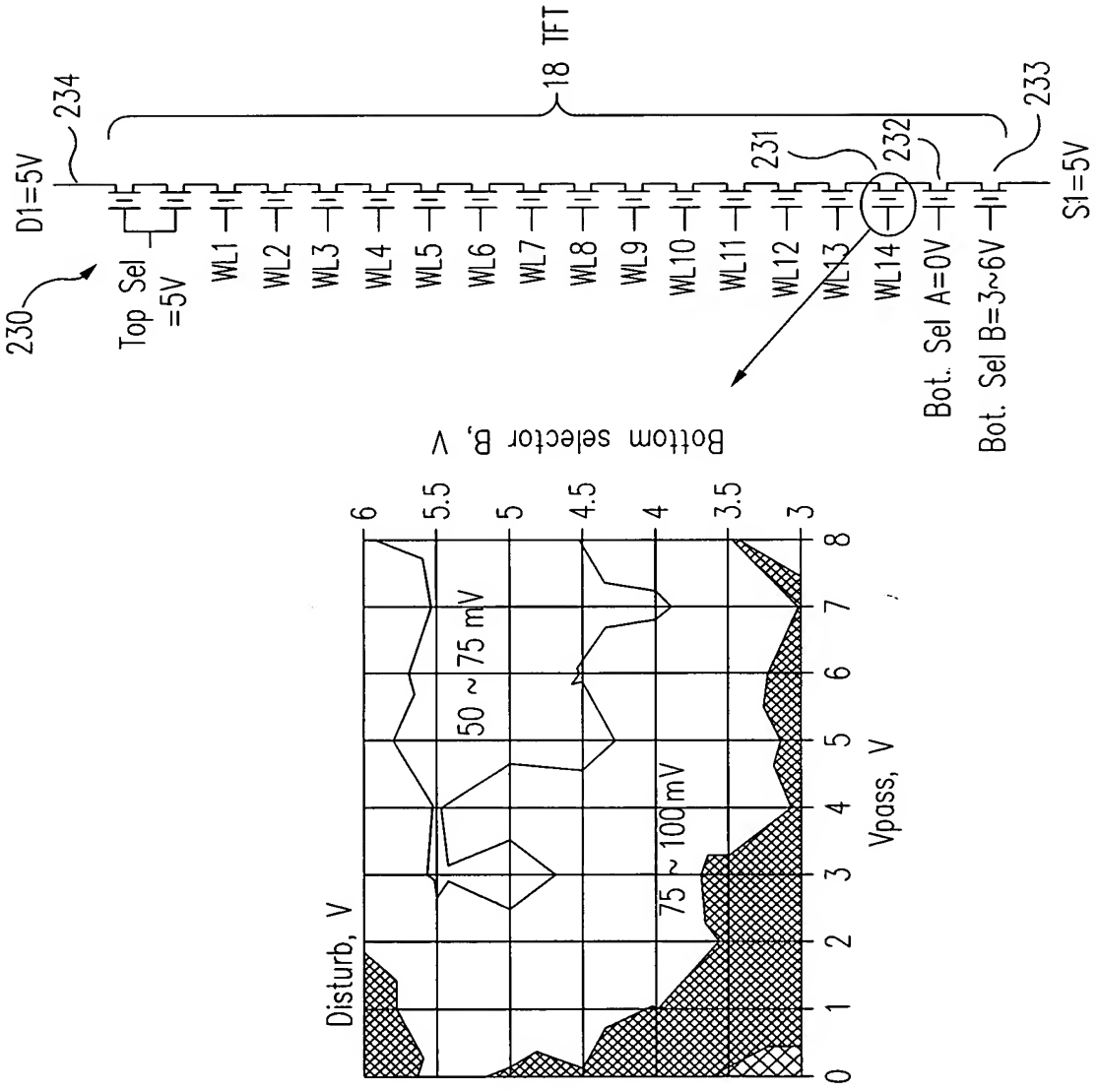
18 TFT
234
233
D1=5V
S1=5V
230
Top Sel =5V
WL1
WL2
WL3
WL4
WL5
WL6
WL7
WL8
WL9
WL10
WL11
WL12
WL13
WL14
231
232
Bot. Sel A=0V
Bot. Sel B=3~6V
Bottom selector B, V
6
5.5
5
4.5
4
3.5
3
50 ~ 75 mV
75 ~ 100 mV
Disturb, V
0 1 2 3 4 5 6 7 8
Vpass, V

FIG. 11

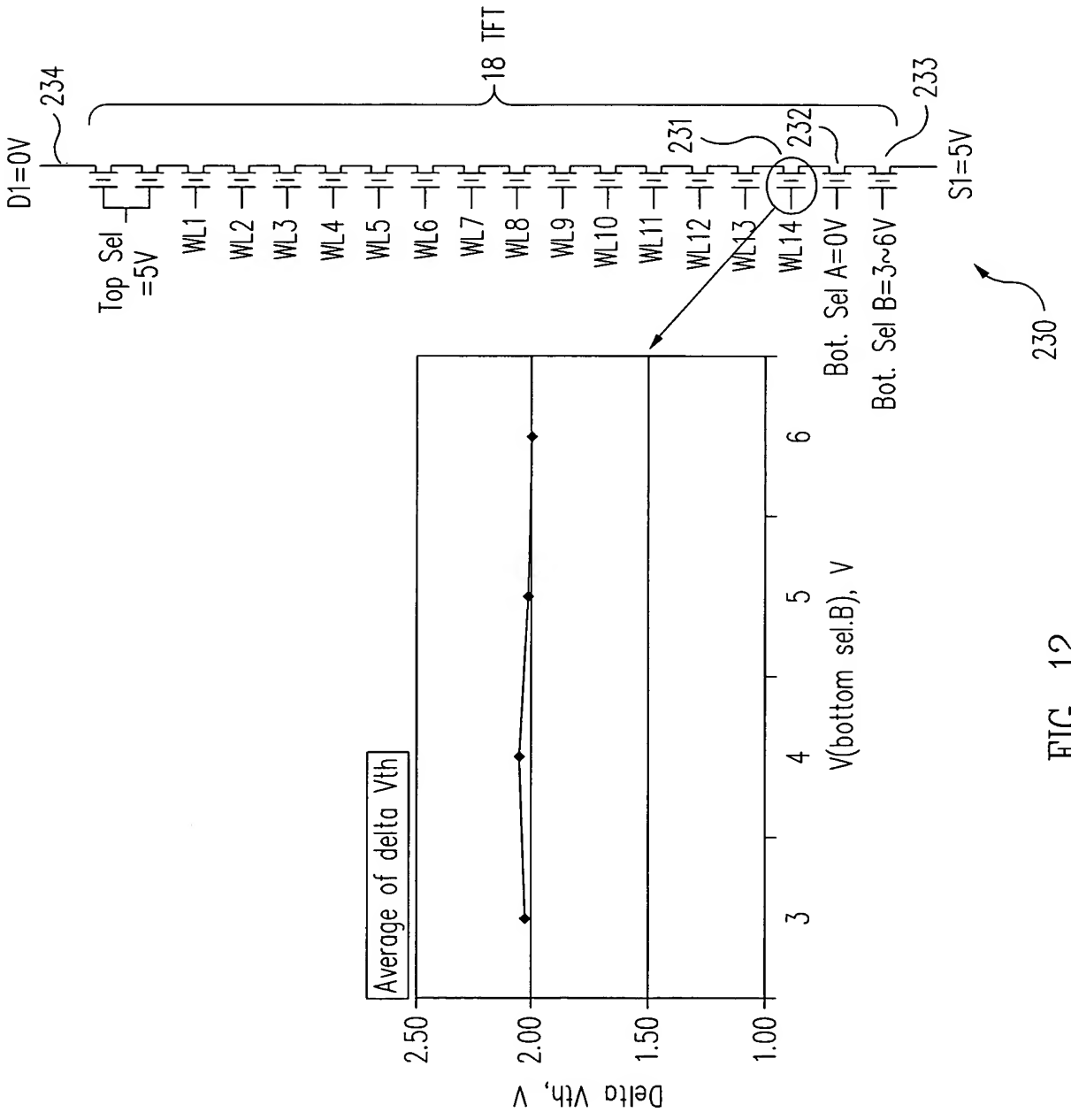
18 TFT
D1=0V
234
Top Sel
=5V
WL1
WL2
WL3
WL4
WL5
WL6
WL7
WL8
WL9
WL10
WL11
WL12
WL13
WL14
231
232
233
Bot. Sel A=0V
Bot. Sel B=3~6V
S1=5V
230
Average of delta Vth
Delta Vth, V
2.50
2.00
1.50
1.00
3
4
5
6
V(bottom sel.B), V

FIG. 12

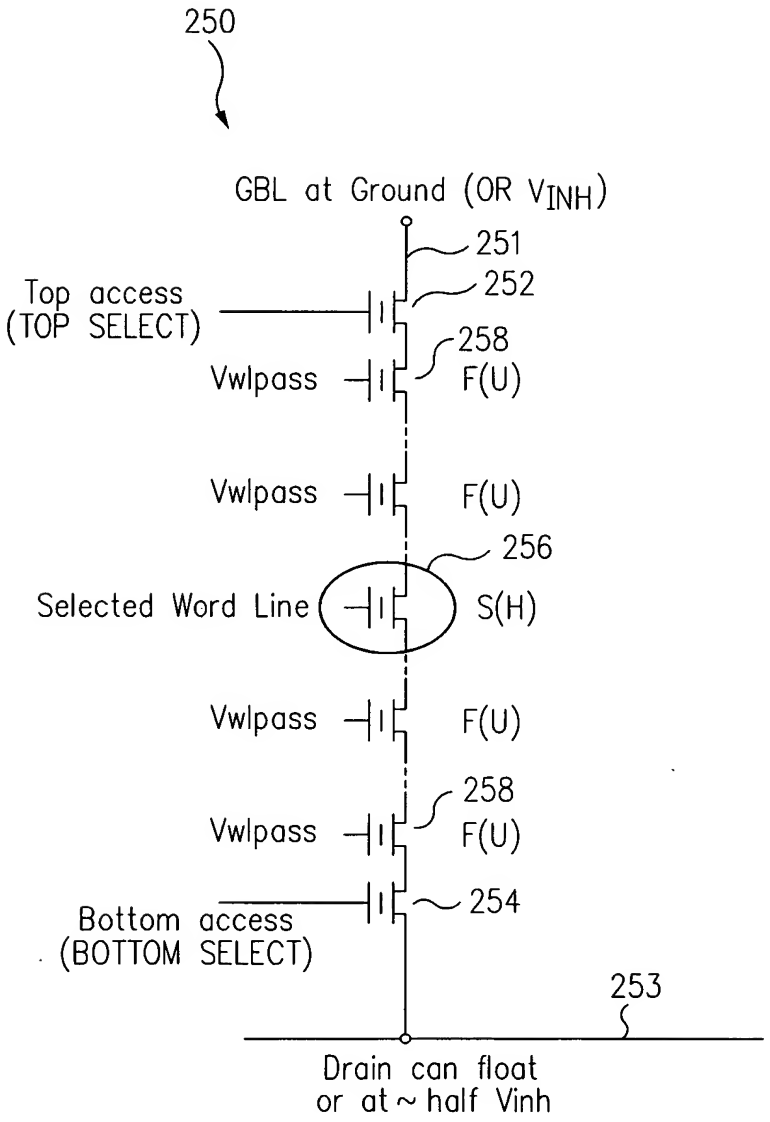
250
GBL at Ground (OR V_{INH})
251
252
Top access
(TOP SELECT)
258
F(U)
Vwlpass
Vwlpass
F(U)
256
Selected Word Line
S(H)
Vwlpass
F(U)
258
Vwlpass
F(U)
254
Bottom access
(BOTTOM SELECT)
253
Drain can float
or at ~ half Vinh

FIG. 13

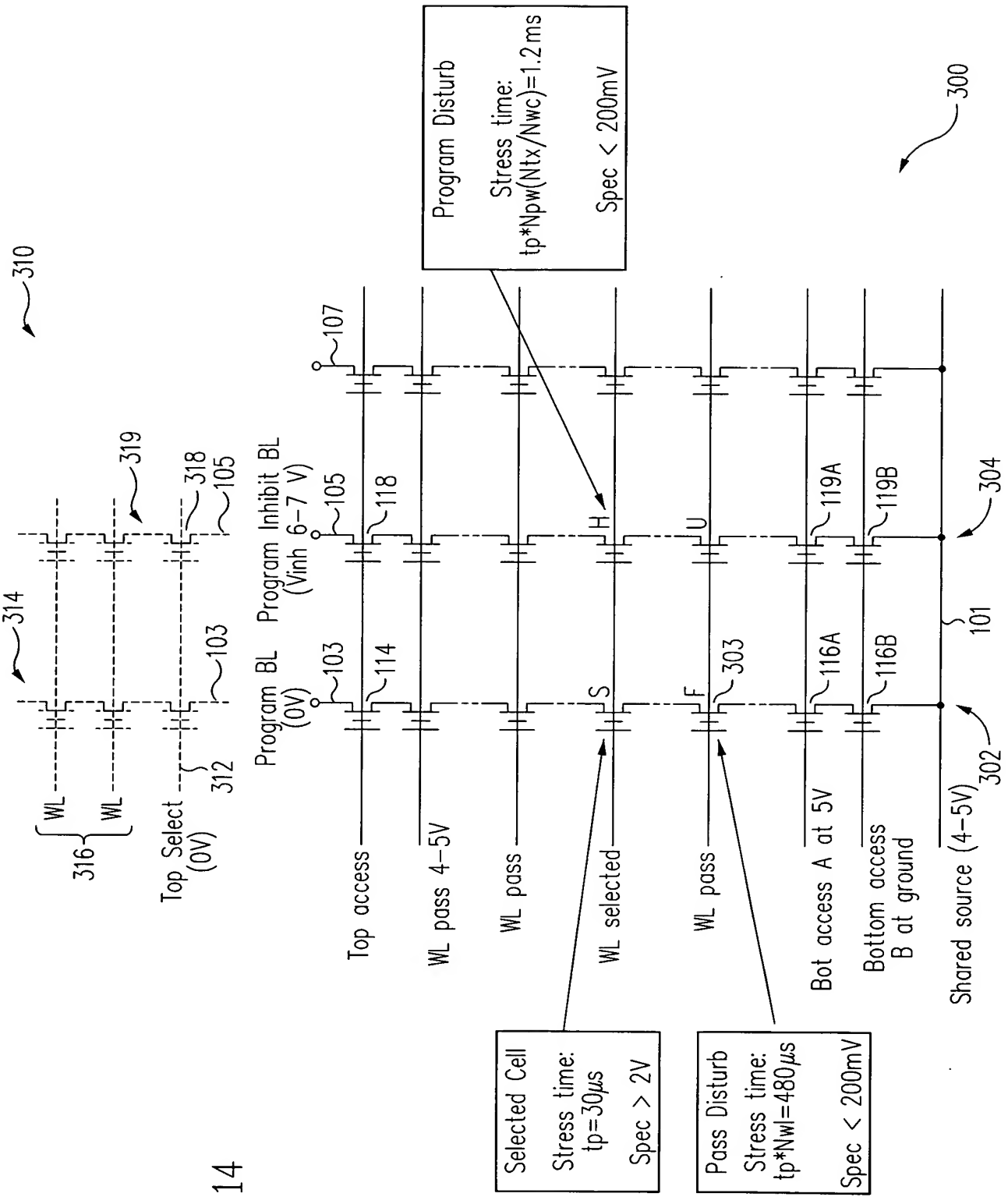
300
310
314
316
WL
WL
319
318
105
103
312
Top Select (0V)
Program BL (0V)
Program Inhibit BL (Vinh 6-7 V)
107
105
118
103
114
Program Disturb
Stress time: tp*Npw(Ntx/Nwc)=1.2 ms
Spec < 200mV
H
U
S
F
303
119A
119B
116A
116B
304
101
302
Top access
WL pass 4-5V
WL pass
WL selected
WL pass
Bot access A at 5V
Bottom access B at ground
Shared source (4-5V)
Selected Cell
Stress time: tp=30μs
Spec > 2V
Pass Disturb
Stress time: tp*Nwl=480μs
Spec < 200mV

FIG. 14

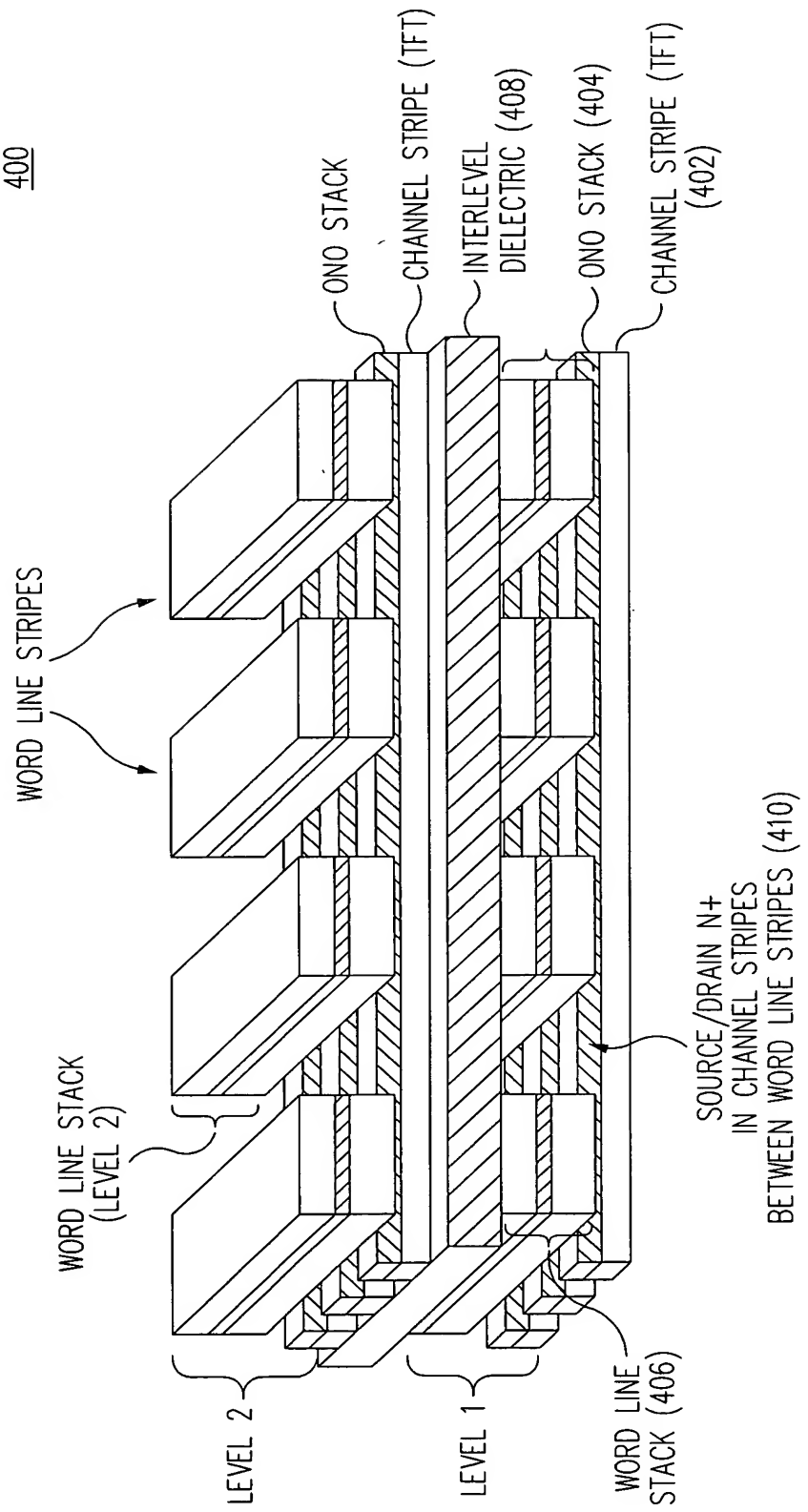
400
ONO STACK
CHANNEL STRIPE (TFT)
INTERLEVEL DIELECTRIC (408)
ONO STACK (404)
CHANNEL STRIPE (TFT) (402)
WORD LINE STRIPES
WORD LINE STACK (LEVEL 2)
SOURCE/DRAIN N+ IN CHANNEL STRIPES BETWEEN WORD LINE STRIPES (410)
LEVEL 2
LEVEL 1
WORD LINE STACK (406)

FIG. 15

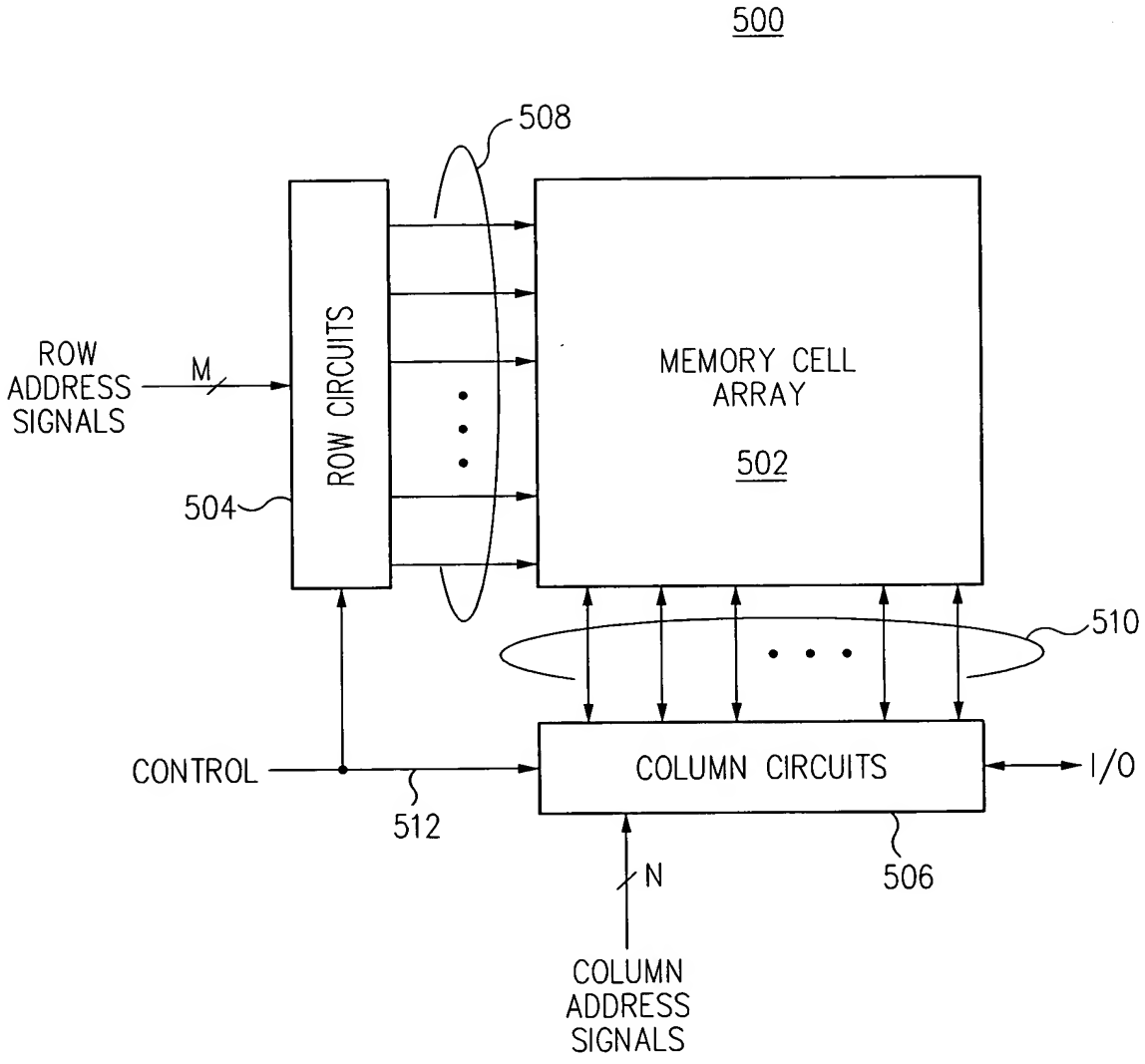
500
508
ROW
ADDRESS
SIGNALS
M
ROW CIRCUITS
504
MEMORY CELL
ARRAY
502
510
CONTROL
512
COLUMN CIRCUITS
I/O
N
506
COLUMN
ADDRESS
SIGNALS

FIG. 16

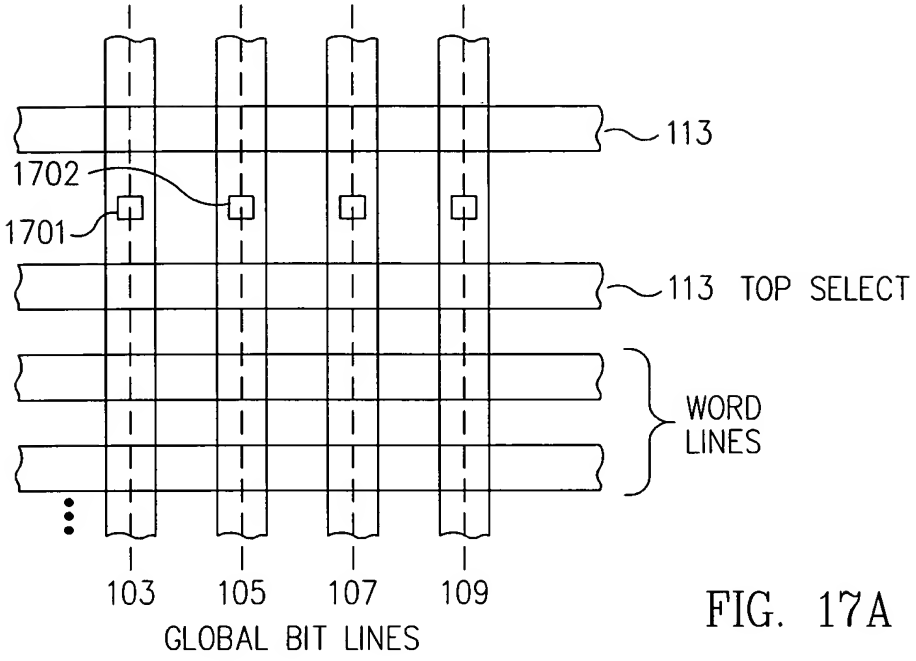

FIG. 17A

GLOBAL BIT LINES 103, 107 ON ONE LAYER
GLOBAL BIT LINES 105, 109 ON 2ND LAYER

FIG. 17B

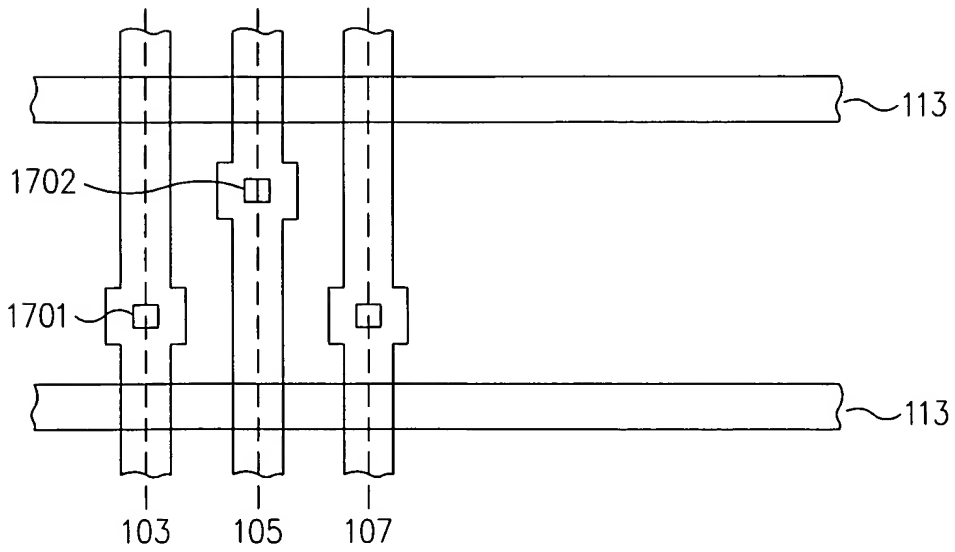

FIG. 17C

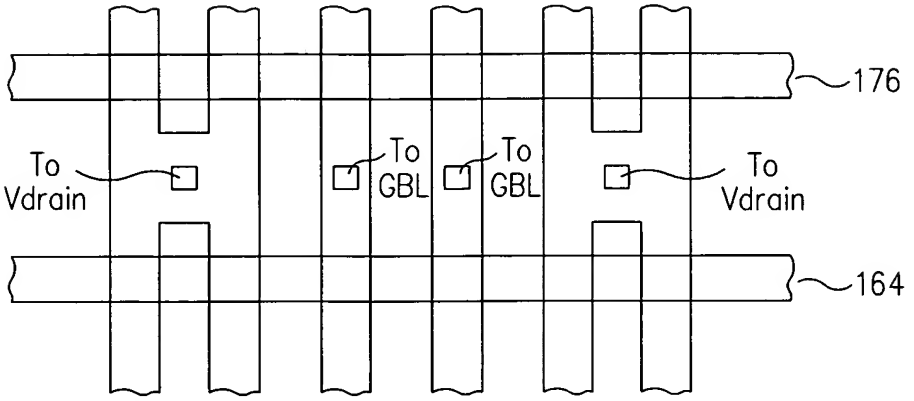

FIG. 17D

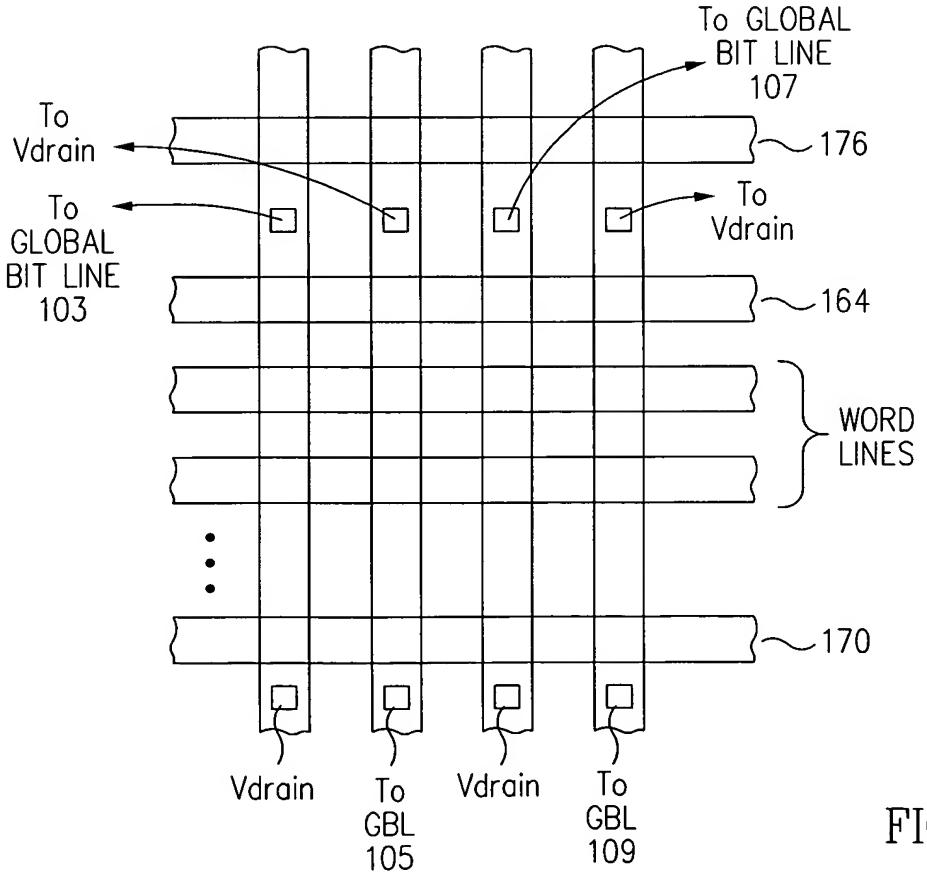

FIG. 17E

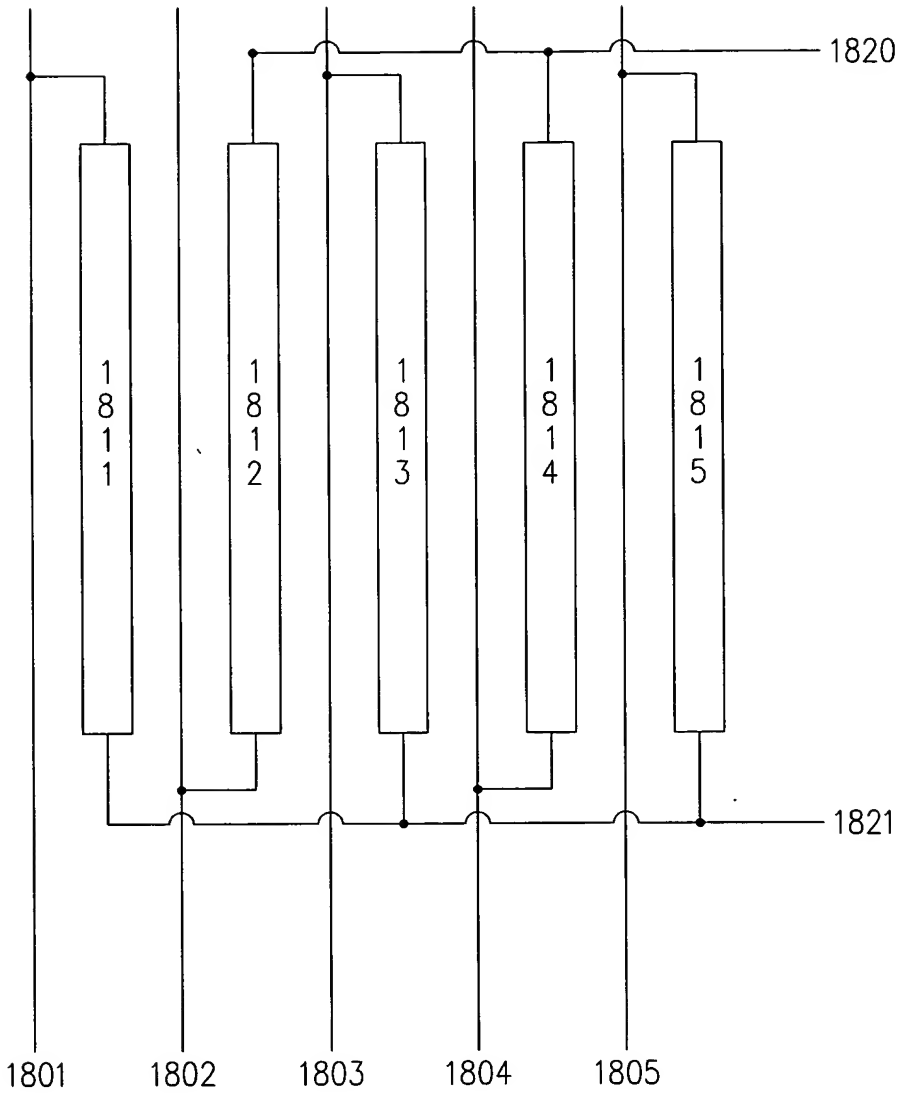

FIG. 18